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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,453	12/24/2001	Paul Gerard D'Arcy	13-1	1909

7590 03/04/2005

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,453	D'ARCY ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/20/2004 have been fully considered but they are not persuasive.

The Applicant contends, "Claim 15 recites that in the Viterbi decoder of claim 12, the add-compare-select algorithm is implemented in accordance with an integrated circuit device. Applicants believe that such claim is not indefinite in any way. By way of example only, it is known that integrated circuits such as digital signal processors (DSPS) can be programmed to implement steps of an algorithm. Further, integrated circuits can be designed and configured to implement steps of an algorithm. Accordingly, Applicants believe that claim 15 is definite".

The Examiner disagrees and asserts that an algorithm is an abstract set of steps independent of any hardware including integrated circuits. The statement "the add-compare-select algorithm is implemented in accordance with an integrated circuit device" implies that the algorithm depends on the integrated circuit. If the applicant intended an integrated circuits "designed and configured to implement steps of an algorithm", then the applicant should explicitly claim that.

The Applicant contends, "However, despite the contention in the Office Action to the contrary, no where does this portion of Yamanaka, nor any other portion of Yamanaka,

disclose that 'substantially concurrent with the respective addition of the input values of the two or more sets of input values, the two or more sets of input values are compared, ' as recited in the claimed invention". The Examiner asserts that even the Applicant recognizes on page 2 lines 10-16 in the Applicant's disclosure recognize that the slowdown in ACS circuitry is due to requiring results from the addition section and that the solution is to provide the same inputs to the compare circuitry and the add circuitry at the same time as in Figure 5 of the Applicant's specification and Figure 6 of Yamanaka. The comparing Sections in Figure 6 of Yamanaka receive the same inputs as the Adders in Figure 6 of Yamanaka at the same time. The comparing Sections and Adding section produce outputs required by Selecting Sections and the outputs are required to arrive at the Selecting Sections at the same time since they are required for operating the Selecting Sections. Yamanaka teaches no delays used in conjunction with either the comparing Sections in Figure 6 of Yamanaka nor the Adders in Figure 6 of Yamanaka nor is it conceivable that Yamanaka would go through such effort to remove the traditional delay found in conventional ACS circuitry and then reintroduce some delay to force the comparing Sections in Figure 6 of Yamanaka and the Adders to operate in a non-parallel fashion.

With regard to claims 2-4, 6, 8, 9, 11, 13, 14, 17, 18, 20 and 21, the Applicant contends, "Applicants respectfully assert that Yamanaka fails to disclose the proper motivation to be modified to yield the claimed invention."

The Examiner disagrees and asserts that lines 5-10, col. 1 of Yamanaka teach that the ACS circuitry is for use in a Viterbi decoder. ACS circuitry is required for the Viterbi algorithm and is used to update path metrics by adding a previous path metric to current branch metrics (see Abstract, Yamanaka). The current path metrics in the Viterbi algorithm are then compared to determine surviving paths (see Abstract, Yamanaka). One of ordinary skill in the art at the time the invention was made would have been highly motivated to use he ACS circuitry of Yamanaka for a Viterbi decoder since that is what Yamanaka designed it for (lines 5-10, col. 1 of Yamanaka).

The Applicant contends, "No where does Yamanaka disclose or even suggest motivation to be modified to provide a comparison operation that comprises performing carry save addition". Col. 13, lines 25-31 in Yamanaka teach that a carry operation is performed at comparator 26 of Figure 18 in Yamanaka (Note: carry is a standard operation in any ACS circuit), storing section 7 and 11 comprise and storage device for storing output of the comparators; hence combined with the comparators and adders comprise carry save addition circuitry for performing carry save addition.

The Applicant contends, "Furthermore, while Yamanaka mentions 4:2 compressors, no where does Yamanaka disclose or even suggest motivation to be modified to provide a comparison operation wherein the carry save addition operation is performed by one or more data compressors, as recited in claim 4".

The Examiner disagrees and asserts that Claim 11 in Yamanaka teaches at least one of said two comparators in Figures 6 and 18 of Yamanaka is a compressor and an arithmetic operation device. Col. 13, lines 25-31 in Yamanaka teach that a carry operation is performed at comparator 26 of Figure 18 in Yamanaka (Note: carry is a standard operation in any ACS circuit), storing section 7 and 11 comprise and storage device for storing output of the comparators; hence combined with the comparators and adders comprise carry save addition circuitry for performing carry save addition.

The Examiner disagrees with the applicant and maintains all rejections of claims 1-21. All amendments and arguments by the applicant have been considered. It is the Examiner's conclusion that claims 1-21 are not patentably distinct or non-obvious over the prior art of record in view of the reference, Yamanaka; Ryutaro et al. (US 6330684 B1, hereafter referred to as Yamanaka) as applied in the last office action, filed 08/11/2004. Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 5, 7, 10, 12, 15, 16 and 19 rejected under 35 U.S.C. 102(e) as being anticipated by Yamanaka; Ryutaro et al. (US 6330684 B1, hereafter referred to as Yamanaka).

See the Non-Final Action filed 08/11/2004 for detailed action of prior rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 2-4, 6, 8, 9, 11, 13, 14, 17, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanaka; Ryutaro et al. (US 6330684 B1, hereafter referred to as Yamanaka).

See the Non-Final Action filed 08/11/2004 for detailed action of prior rejections.

Conclusion

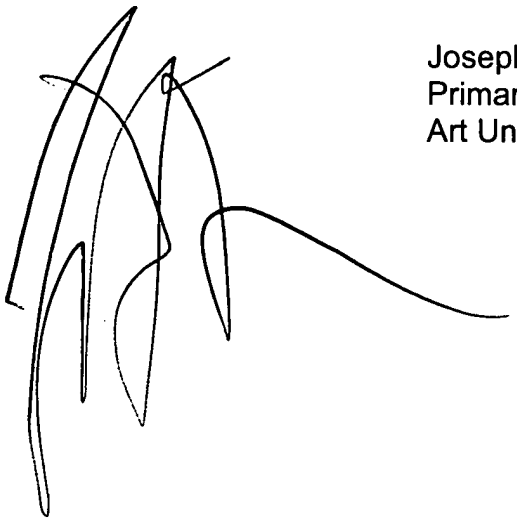
4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133